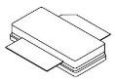
1300MHz-1700MHz, 230W, 28V High Power RF LDMOS FETs

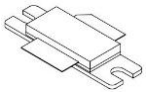
Description

The ITCH16230B2 is a 230-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 1300 to 1700 MHz. It Can be used in Class AB/B and Class C for all typical cellular base station modulation formats.

ITCH16230B2



ITCH16230B2E



•Typical Performance (On Innogration fixture with device soldered):

VDD = 28 Volts, I_{DQ} = 100 mA,CW.

Frequency	Gp (dB)	P_{OUT} (W)	η_D@ (%)
1470 MHz	16.5	240	62.2
1500 MHz	15.9	214	62.1
1525 MHz	15.4	191	62.4

•Typical Performance (On Innogration fixture with device soldered):

VDD = 28 Volts, Vgs=2.7V, I_{DQ} = 900 mA, pulse width 12us, duty cycle 10%

Frequency	Linear Gain (dB)	P_{1dB}(dBm)	P_{3dB}(dBm)	P_{3dB}(W)	η_D@P_{3dB} (%)
1350 MHz	17.5	54.3	55	315	58.1
1375 MHz	18	53.86	54.6	288	58.3
1400 MHz	18.5	53.34	54	256	58.8

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.32	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 900 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.7	3.2	V
Functional Tests (In Innogration 1.35-1.4GHz-demo, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 900 mA, f = 1400 MHz, pulse width 12us, duty cycle 10% .					
Linear Gain	Gp	17.5	18.5		dB
Power Out	P_{OUT}	230	256		W
Drain Efficiency@ P_{OUT}	η_D	54	58		%
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 800 mA, f = 1500 MHz

VSWR 10:1 at 230W pulse CW Output Power	No Device Degradation

Figure 1: Power sweep curve (1350-1400MHz)

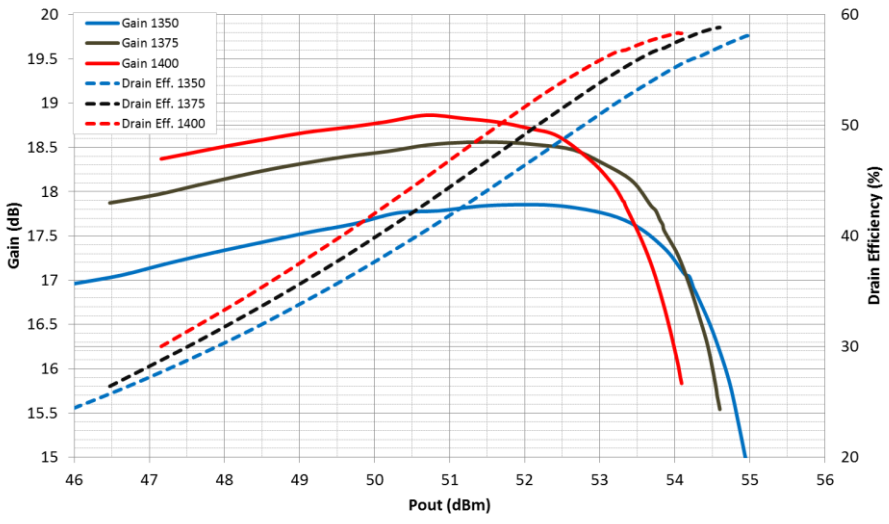


Photo of the test circuit(1350-1400MHz)

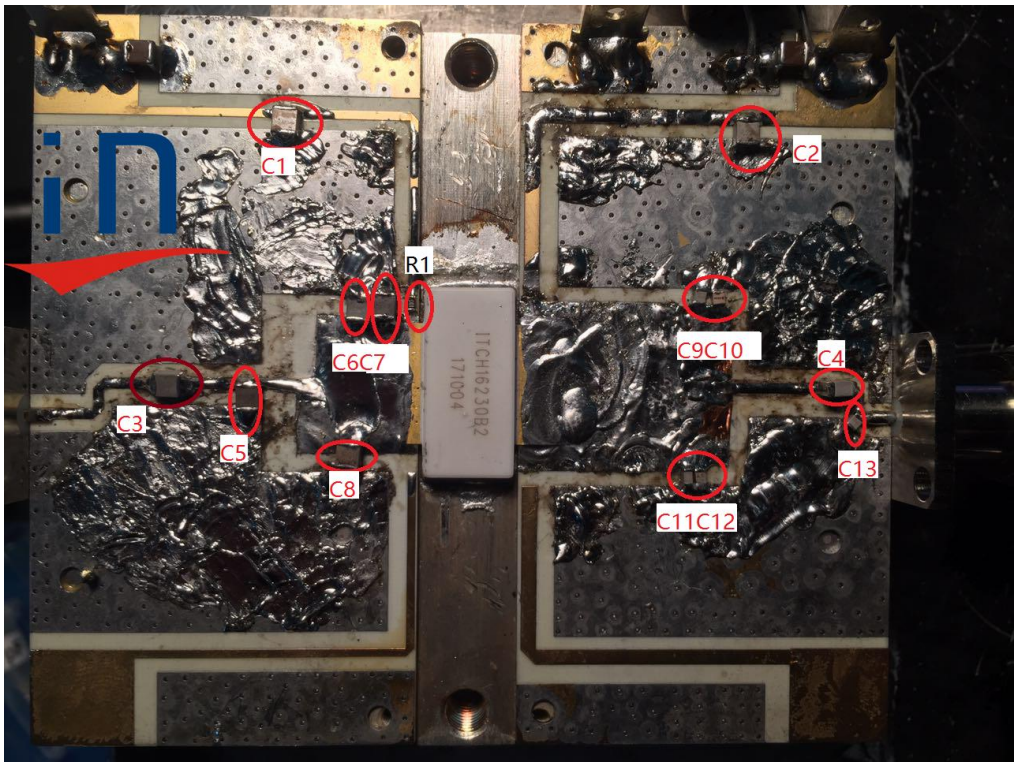
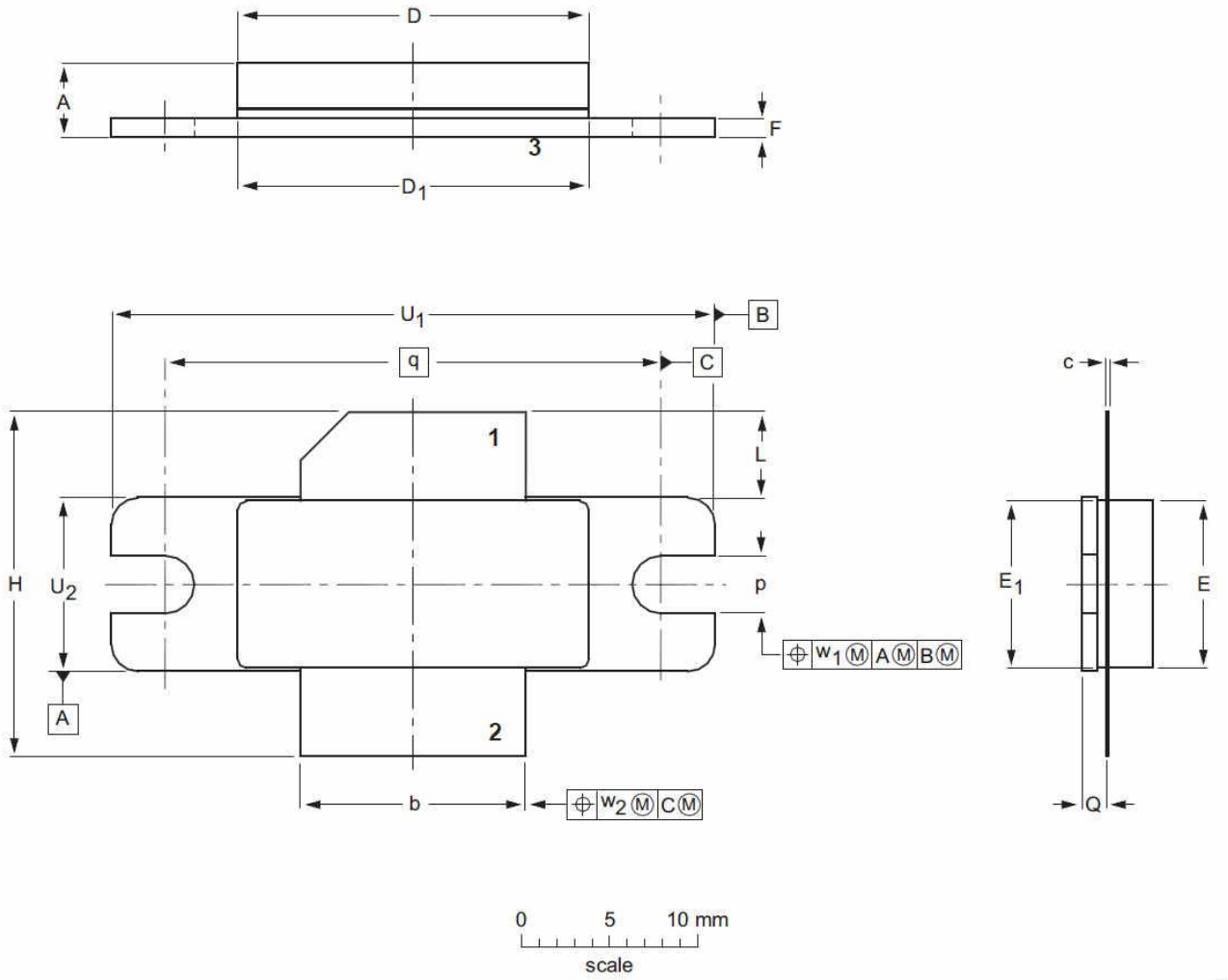


Table 5: BOM of Test Circuit(1350-1400MHz)

Component	Value	Description
R1	10 Ω	0603
C1	56 pF	ATC600F
C2	27 pF	ATC600F
C3	30 pF	ATC600F
C4	27 pF	ATC600F
C5	3.3 pF	ATC600F
C6	1.8 pF	ATC600F
C7	2.7 pF	ATC600F
C8	1.5 pF	ATC600F
C9	1.0 pF	ATC600F
C10	1.5 pF	ATC600F
C11	1.4 pF	ATC600F
C12	1.0 pF	ATC600F
C13	0.9 pF	ATC600F

Package Outline

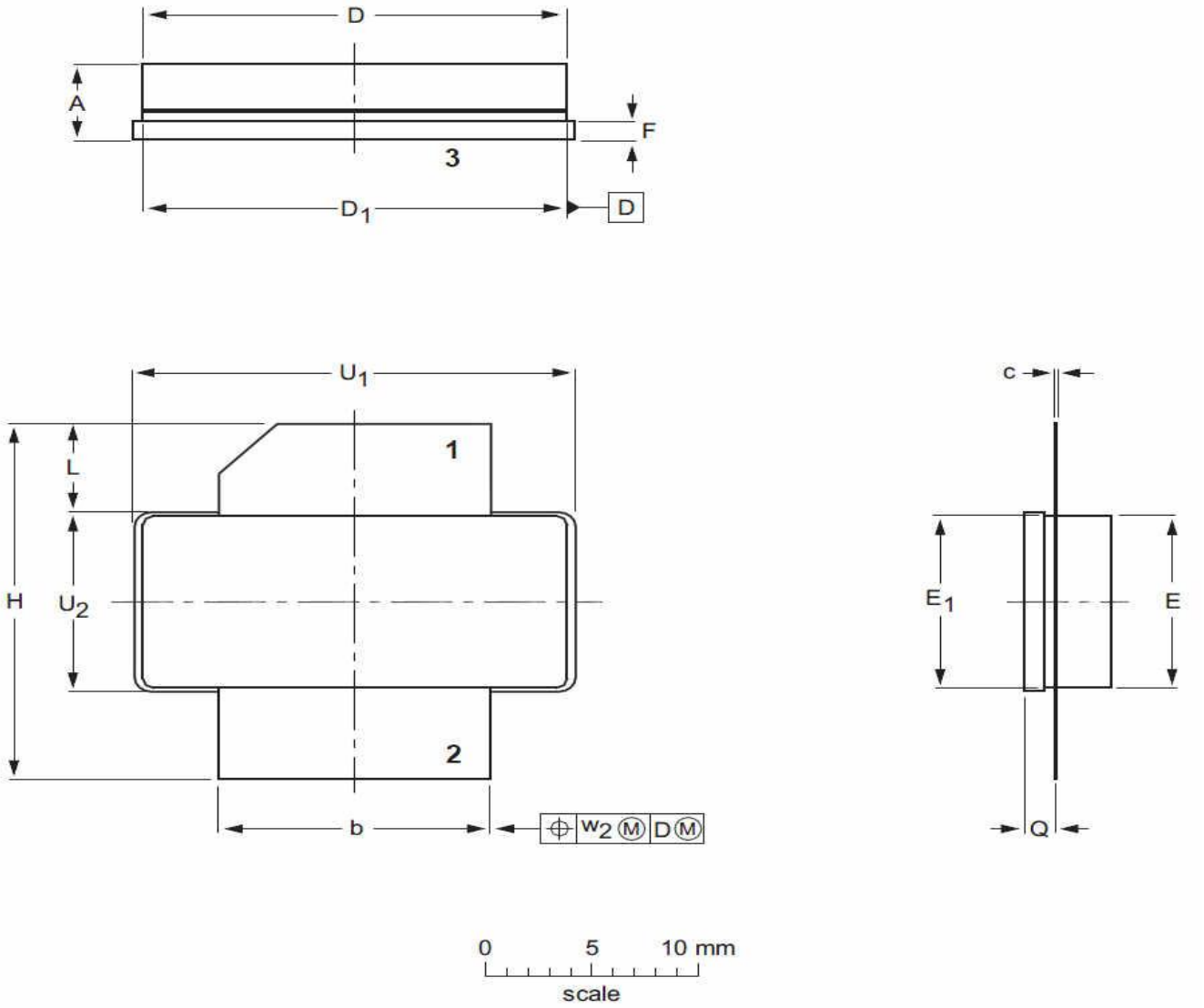
Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
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inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/02/23	Rev 1.0	Preliminary Datasheet V1.0
2017/04/5	Rev 1.1	Modify 1350-1400MHz performance and test curve

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